**What is claimed is:**

1. An interface for receiving data from an image sensor having an imaging array and a clock generator for transfer to a processor system comprising:
   - memory means for storing imaging array data and clocking signals at a rate determined by the clocking signals;
   - signal generator means for generating a signal for transmission to the processor system in response to the quantity of data in the memory means; and
   - circuit means for controlling the transfer of the data from the memory means at a rate determined by the processor system.

2. An interface as claimed in claim 1 wherein the memory means is a first-in first-out (FIFO) buffer.

3. An interface as claimed in claim 2 wherein the signal generator means generates an interrupt signal for transmission to the processor system.

4. An interface as claimed in claim 3 wherein the circuit means for controlling the transfer of the data includes:
   - command decoder means for receiving address and command signals from the processor system;
   - configuration register means for storing configuration data for the FIFO buffer; and
   - read control means for controlling the read-out of the FIFO buffer.

5. An interface as claimed in claim 4 wherein the interface further includes array register means for determining the dimension of the imaging array data.

6. An interface as claimed in claim 2 wherein the signal generator means generates a bus request signal for transmission to a bus arbitration unit for the processor system.

7. An interface as claimed in claim 6 wherein the circuit means for controlling the transfer of the data further includes:

- command decoder means for receiving address and command signals from the processor system;
- configuration register means storing configuration data for the FIFO buffer;
- read control means for controlling the read-out of the FIFO buffer; and
- bus command unit means for receiving control of the system bus and providing an address for the data read-out from the buffer means.

8. An interface as claimed in claim 1 wherein the memory means is an addressable memory.

9. An interface as claimed in claim 8 wherein the signal generator means generates an interrupt signal for transmission to the processor system.

10. An interface as claimed in claim 9 wherein the circuit means for controlling the transfer of the data includes:

- command decoder means for receiving address and command signals from the processor system;
- configuration register means for storing configuration data for the addressable memory; and
- read control means for controlling the read-out of the addressable memory.

11. An interface as claimed in claim 10 wherein the interface further includes array register means for determining the dimension of the imaging array data.

12. An interface as claimed in claim 8 wherein the signal generator means generates a bus request signal for transmission to a bus arbitration unit for the processor system.

13. An interface as claimed in claim 12 wherein the circuit means for controlling the transfer of the data further includes:

- command decoder means for receiving address and command signals from the processor system;
- configuration register means storing configuration data for the addressable memory;
- read control means for controlling the read-out of the addressable memory; and
- bus command unit means for receiving control of the system bus and providing an address for the data read-out from the addressable memory.

14. An interface as claimed in claim 13 wherein the interface further includes array register means for determining the dimension of the imaging array data.

15. An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus comprising:

- an imaging array sensor having an array of sensing pixels and an array address generator integrated on a die; and
- interface means integrated on the die for receiving data from the imaging array sensor as determined by the imaging array sensor and adapted to transfer the data to the electronic processing system as determined by the electronic processing system.

16. An integrated semiconductor imaging circuit as claimed in claim 15 where the interface means includes:

- memory means for storing imaging array data and address signals at a rate determined by the imaging array sensor; and
- circuit means for controlling the transfer of the data from the memory means to the data bus at a rate determined by the electronic processing system.

17. An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory means includes a first-in first-out (FIFO) buffer.

18. An integrated semiconductor imaging circuit as claimed in claim 17 which further includes bus arbitration means coupled to the circuit means for controlling the transfer of the data.

19. An integrated semiconductor imaging circuit as claimed in claim 17 which further includes bus arbitration means integrated on the die and coupled to the circuit means for controlling the transfer of the data.

20. An integrated semiconductor imaging circuit as claimed in claim 16 wherein the memory means includes an addressable memory.

21. An integrated semiconductor imaging circuit as claimed in claim 20 which further includes bus arbitration means coupled to the circuit means for controlling the transfer of the data.

22. An integrated semiconductor imaging circuit as claimed in claim 20 which further includes bus arbitration means integrated on the die and coupled to the circuit means for controlling the transfer of the data.

23. An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus comprising:

- an imaging array of sensing pixels;
- buffer means for storing data received at an input port and for outputting data through an output port to the data bus;
- means for transferring data from a selected pixel to the buffer input port;
- means for determining the quantity of data in the buffer means;
- means for alerting the electronic processing system when the quantity

of data in the buffer means attains a predetermined level; and

- means adapted to respond to the electronic processing system for controlling the transfer of the stored data through the buffer means output port.

24. An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus and a system address/control bus comprising:

- an imaging array of sensing pixels;
- buffer means for storing data received at an input port and for outputting data through an output port to the data bus;
- means for transferring data from a selected pixel to the buffer input port;
- means for determining the quantity of data in the buffer means;
- means for seeking control of the data bus when the quantity of data in the buffer means attains a predetermined level; and
- means adapted to respond to the availability of the data bus for controlling the transfer of the stored data through the buffer means output port.

25. An integrated semiconductor imaging circuit as claimed in claim 24 which includes bus arbitration unit means for receiving data bus control requests and for providing data bus control in response to a request.

26. An integrated semiconductor imaging circuit as claimed in claim 25 wherein the means for responding to the availability of the data bus includes:

- means for storing and incrementing destination addresses; and
- means for asserting the destination address and write controls on the system address/control bus.

27. An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus comprising:

- an imaging array of sensing pixels;
- memory means having a plurality of memory cells arranged in rows and columns for storing data received at an input port and for outputting data through an output port to the data bus;
- means for transferring data from a selected pixel to a selected memory cell through the memory means input port;
- means for determining the quantity of data in the memory means;
- means for alerting the electronic processing system when the quantity of data in the memory means attains a predetermined level; and
- means adapted to respond to the electronic processing system for controlling the transfer of the stored data through the memory means output port.

28. An integrated semiconductor imaging circuit for use with an electronic processing system having a data bus and a system address/control bus comprising:

- an imaging array of sensing pixels;
- memory means having a plurality of memory cells arranged in rows and columns for storing data received at an input port and for outputting data through an output port to the data bus;
- means for transferring data from a selected pixel to a selected memory cell through the memory input port;
- means for determining the quantity of data in the memory means;
- means for seeking control of the data bus when the quantity of data in the memory means attains a predetermined level; and
- means adapted to respond to the availability of the data bus for controlling the transfer of the stored data through the memory means output port.

29. An integrated semiconductor imaging circuit as claimed in claim 24 which includes bus arbitration unit means for receiving data bus control requests and for providing data bus control in response to a request.

30. An integrated semiconductor imaging circuit as claimed in claim 25 wherein the means for responding to the availability of the data bus includes:

- means for storing and incrementing destination addresses; and
- means for asserting the destination address and write controls on the system address/control bus.